Utopium

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- MCU8051 processor
 - Several asynchronous examples
 - 256 instructions
 - Some reather complex
 - 256 bytes of ram with memory mapped:
 - Register bank + stack pointer
 - Accumulator, status flags
 - Bit addressable regions
- Started development on February 1st

	8051 Instruction Set Table						@R0	@R1	R0	R1	R2	R3	R4	R5	R6	R7	
Mates (c) 1995, 2002	0000	0001	0010	.3	.4	⁰¹⁰¹ .5	°.6	01117	8.	.9	1010 A	¹⁰¹¹ B	1100 C	1101 D	1110 F	¹¹¹¹ F	
	0 1c 1	1 20 2	2 2c 3	3 1c 1	4 1c 1	5 1c 1	6 1c 1	7 1c 1	8 1c 1	9 1c 1	10 1c 1	11 1c 1	12 1c 1	13 1c 1	14 10 1	15 1c 1	o
10	NOP	AJMP 0A8	LJMP A16	RR A	INC A	INC A8	INC @R0	INC @R1	INC RO	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7	Š
1	16 2c 3	17 2c 2	18 2c 3	19 1c 1	20 1c 1	21 1c 1	22 1c 1	23 1c 1	24 1c 1	25 1c 1	26 1c 1	27 1c 1	28 1c 1	29 1c 1	30 1c 1	31 1c 1	U
11	JBC BIT,AR	ACALL DAS	LCALL A16	RRC A	DECA	DEC A8	DEC @RO	DEC @R1	DEC RO	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7	DE
2	32 2c 3	33 2c 2	34 2c 1	35 1c 1	36 1c 2	37 1c 2	38 1c 1	39 1c 1	40 1c 1	41 1c 1	42 1c 1	43 1c 1	44 1c 1	45 1c 1	46 1c 1	47 1c 1	0
1	JB BIT, AR	AJMP 1A8	RET	RL A	ADD A,#D	ADD A,A8	ADD A,@R0	ADD A,@R1	ADD A,R0	ADD A,R1	ADD A,R2	ADD A,R3	ADD A,R4	ADD A,R5	ADD A,R6	ADD A,R7	₽
2	48 2c 3	49 2c 2	50 2c 1	51 1c 1	52 1c 2	53 1c 2	54 1c 1	55 1c 1	56 1c 1	57 1c 1	58 1c 1	59 1c 1	60 1c 1	61 1c 1	62 1c 1	63 1c 1	8
3	JNB BIT,AR	ACALL 1A8	RETI	RLC A	ADDC A,#D	ADDC A, A8	ADDC A,@R0	ADDC A,@R1	ADDC A,R0	ADDC A,R1	ADDC A,R2	ADDC A,R3	ADDC A,R4	ADDC A,R5	ADDC A,R6	ADDC A,R7	-
1	64 2c 2	65 2c 2	66 1c 2	67 1c 3	68 1c 2	69 1c 2	70 1c 1	71 1c 1	72 1c 1	73 1c 1	74 1c 1	75 1c 1	76 1c 1	77 1c 1	78 1c 1	79 1c 1	RL
4	JC AR	AJMP 2A8	ORL A8,A	ORL A8,#D	ORL A,#D	ORL A,A8	ORL A,@R0	ORL A,@R1	ORL A,R0	ORL A,R1	ORL A,R2	ORL A,R3	ORL A,R4	ORL A,R5	ORL A,R6	ORL A,R7	ō
5	80 2c 2	81 2c 2	82 1c 2	83 1c 3	84 1c 2	85 1c 2	86 1c 1	87 1c 1	88 1c 1	89 1c 1	90 tc 1	91 1c 1	92 1c 1	93 1c 1	94 1c 1	95 1c 1	ANL
J	JNC AR	ACALL 2A8	ANL AS	ANL A8,#D	ANL A,#D	ANL A,A8	ANL A,@R0	ANL A,@R1	ANL A,R0	ANL A,R1	ANL A,R2	ANL A,R3	ANL A,R4	ANL A,R5	ANL A,R6	ANL A,R7	¥
6	96 2c 2	97 2c 2	98 1c 2	99 1c 3	100 1c 2	101 10 2	102 1c 1	103 1c 1	104 1c 1	105 1c 1	106 1c 1	107 1c 1	108 1c 1	109 1c 1	110 1c 1	111 1c 1	占
U	JZ AR	AJMP 3A8	XRL A8,A	XRL A8,#D	XRL A,#D	XRL A,A8	XRL A,@R0	XRL A,@R1	XRL A,R0	XRL A,R1	XRL A,R2	XRL A,R3	XRL A,R4	XRL A,R5	XRL A,R6	XRL A,R7	×
7	112 2c 2	113 20 2	114 2c 2	115 26 1	116 1c 2	117 2c 3	118 1c 2	119 1c 2	120 1c 2	121 1c 2	122 1c 2	123 2c 2	124 1c 2	125 1c 2	126 1c 2	127 1c 2	6
	JNZ AR	ACALL 3A8	ORL C,BIT	JMP @A+DPTR	MOV A,≢D	MOV A8,#D	MOV @R0,#D	MOV @R1,#D	MOV R0,#D	MOV R1,#D	MOV R2,#D	MOV R3,#D	MOV R4,#D	MOV R5,#D	MOV R6,#D		Z
8	128 26 2	129 2c 2	130 2c 2	131 2c 1	132 4c 1	133 2c 3	134 2c 2	135 2c 2	136 2c 2	137 2c 2	138 2c 2	139 2c 2	140 2c 2	141 2c 2	142 2c 2	Charles Control (con	6
0	SJMP AR	AJMP 4A8	ANL C, BIT	MOVC A,@A+PC	DIV AB	Property of the Contract of	MOV A8,@R0			MOV A8,R1	Comment of the Commen				A STATE OF THE STA	MOV A8,R7	100
9	144 20 3	145 2c 2	146 2c 2	147 20 1	148 1c 2	149 1c 2	150 1c 1	151 1c 1	152 1c 1	153 1c 1	154 1c 1	155 1c 1	156 1c 1	157 1c 1	158 1c 1	159 1c 1	188
J	CANTON STORY	ACALL 4A8	The second second second	MOVC A,@A+DPTR			SUBB A,@R0	STATE OF THE PERSON NAMED IN COLUMN		SUBB A,R1	BURNOWN DOWNER DOWN	Control of the last	STATE OF THE PARTY	The second second second	SCHOOL SERVICE STATE	AND DESCRIPTION OF THE PERSON	
Δ		161 2c 2	162 1c 2	The same of the sa	164 4c 1	165		167 2c 2	168 2c 2		170 2c 2		172 2c 2			175 2c 2	10
	ORL C,BIT	AJMP 5A8	MOV C,BIT	BOULEST-CHILD IN	MULAB		The second second second	100000000000000000000000000000000000000	AND DESCRIPTIONS OF A	MOV R1,A8	Maria de la companya del companya de la companya del companya de la companya de l	ingenteen geven en vervee	ACRESHAN PRODUCES CONTRACTOR	CARLO CONTRACTOR	Contract of the Contract of th	Control of the Control	100
B		177 2c 2	178 1c 2		CONTRACTOR CONTRACTOR	181 20 3	DOMESTIC TO SERVICE TO	183 2c 3		185 2c 3				277			
ш	means less less	ACALL 5A8	CPL BIT	CPLC	immediates and with AND for	CJNE A,A8,AR		CJNE @R1,#D,AR	BEAD OF STREET	ENGINEERS (SEE SEE	TOTAL PROPERTY.	Hazarota Parito Policio de	- The second second second	200000000000000000000000000000000000000	550000000000000000000000000000000000000	STATE OF STREET	-
	192 2c 2	193 2c 2	194 1c 2	0.000 (0.000)	196 1c 1	197 1c 2	grossysandmine (direct	199 1c 1	200 1c 1	201 1c 1	South Section Co.	Testing of the second	And the following of the con-	205 1c 1	206 1c 1	Service Constitution	O
\vdash	PUSH A8	AJMP 6A8	CLR BIT	CLR C	SWAP A	XCH A,A8	XCH A,@R0		XCH A,R0	XCH A,R1	XCH A,R2	XCH A,R3	XCH A,R4	XCH A,R5	XCH A,R6	XCH A,R7	×
	208 2c 2	209 20 2	210 1c 2	2000	212 1c 1	213 20 3	214 1c 1		216 2c 2	CONTRACT DESCRIPTION	CONTRACTOR DESCRIPTION OF THE PERSON NAMED IN CONTRACTOR OF THE PERSON NAM	219 2c 2	SCHOOL SECTION	Parameter Company (Sec.)	Participated Sections (Section)	223 2c 2	-
12	POP A8	ACALL 6A8	-Consideration (CV)	SETB C	DAA	The same of the sa				DJNZ R1,AR	Control of the Contro	THE RESERVE OF THE PARTY OF THE	Charles Section 2000	Service Control of the Control of th	STATE OF THE PARTY	100000000000000000000000000000000000000	-
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	MOVX A,@DPTR	AJMP 7A8	MOVX A,@R0		CLR A	Annual Control of the	MOV A,@R0		MOV A,R0	MOV A,R1	MOV A,R2	Company of the Compan	MOV A,R4	MOV A,R5		Contract of the	N
	240 2c 1	241 2c 2	242 2c 1		244 1c 1	245 1c 2	246 1c 1		248 1c 1	249 1c 1	250 1c 1	251 1c 1	252 1c 1	253 1c 1	254 1c 1	255 1c 1	10
	MOAY GOLIK'Y	ACALL 7A8	MOVX @R0,A	MUVA @K1,A	CPL A	MOV A8,A	MOV @R0,A	MUV @K1,A	MOV RU,A	MOV R1,A	MOV R2,A	MOV K3,A	MOV R4,A	MOV R5,A	MOV R6,A	MOV R7,A	Z

A16 ... address 16 bits BIT ... bit's address

A8 address 8 bits AR relative address 8 bits

D, data 8 bits D16 ... data 16 bits Code Cycles Bytes INSTRUCTION

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February 6th

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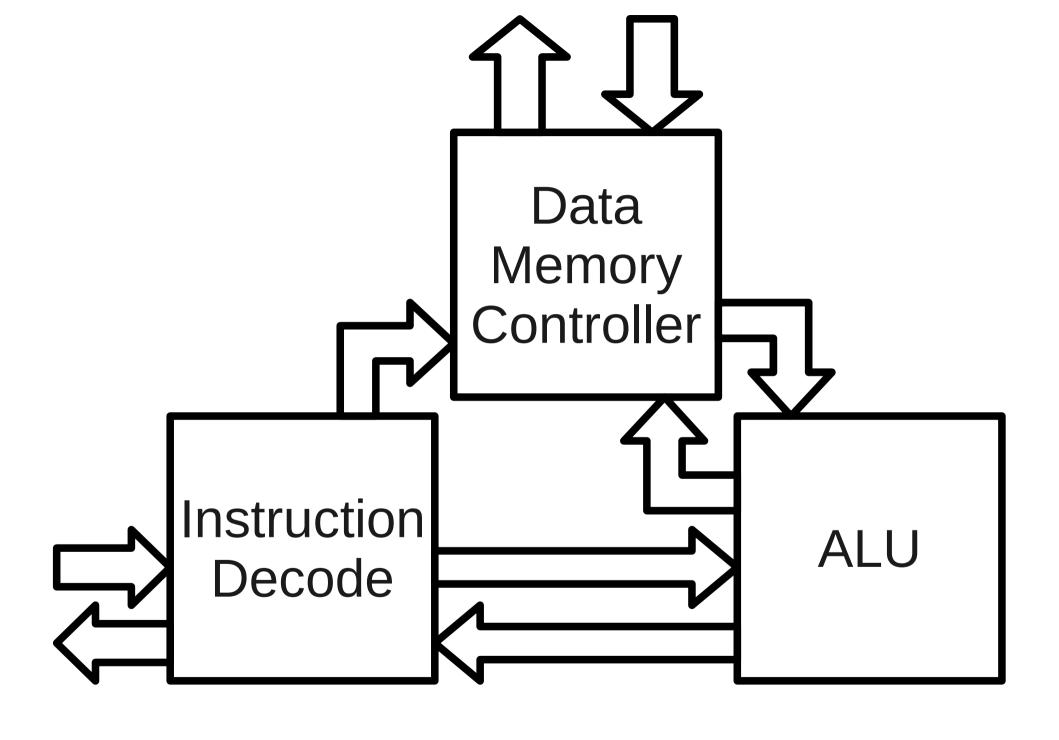


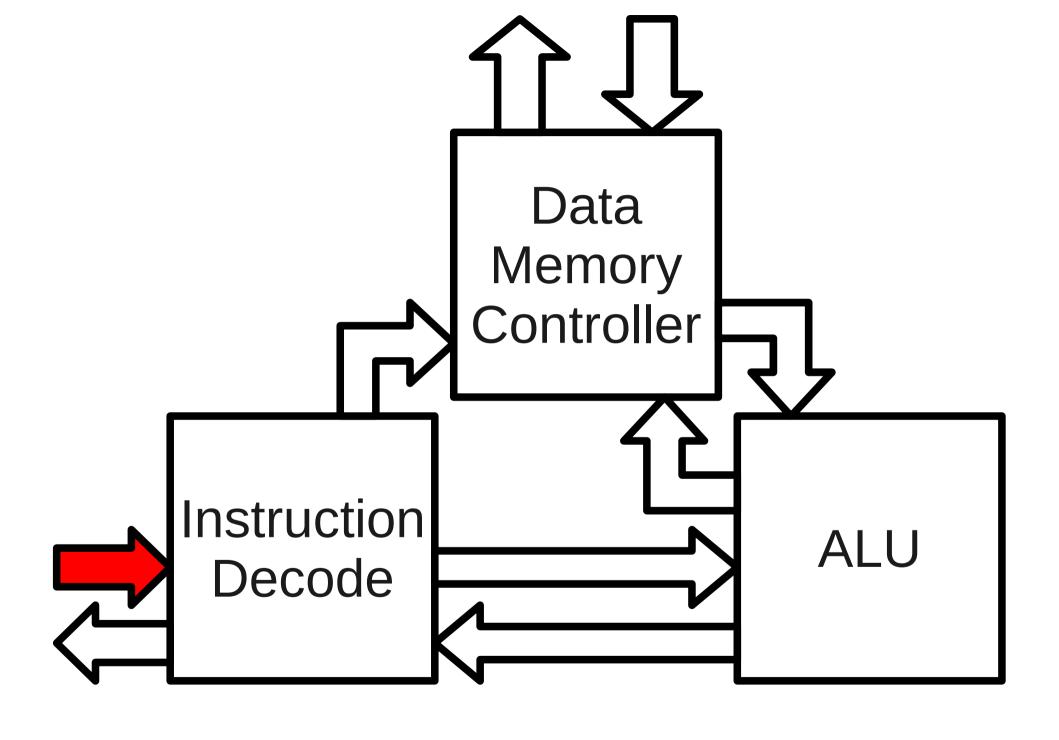
February 13th

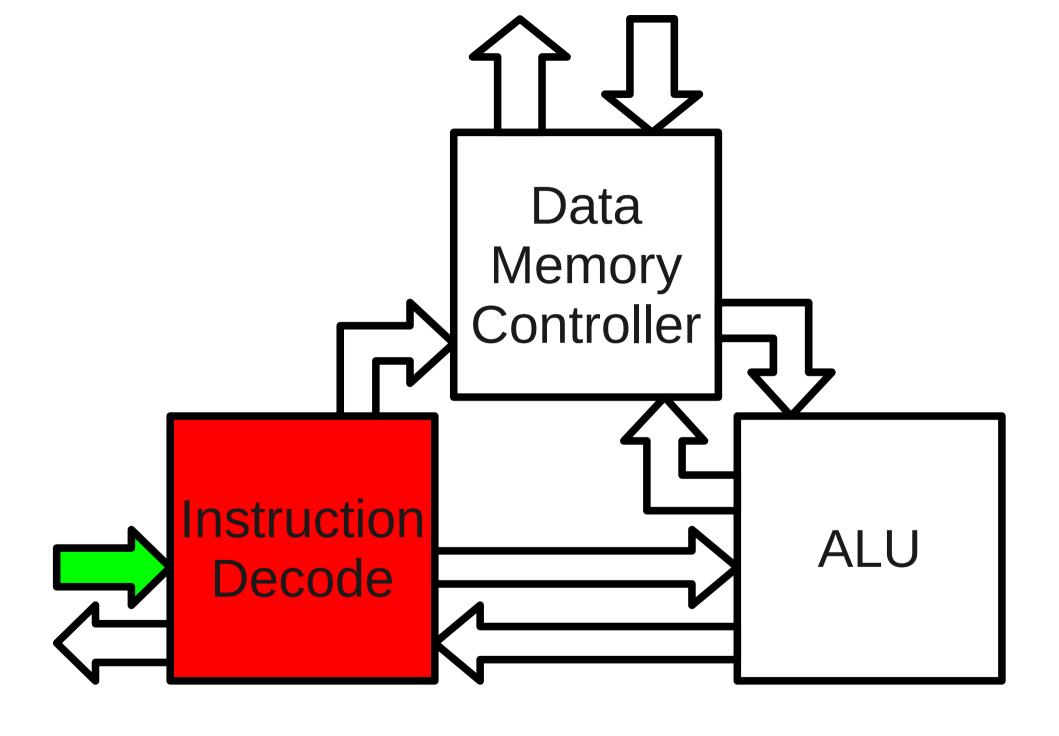


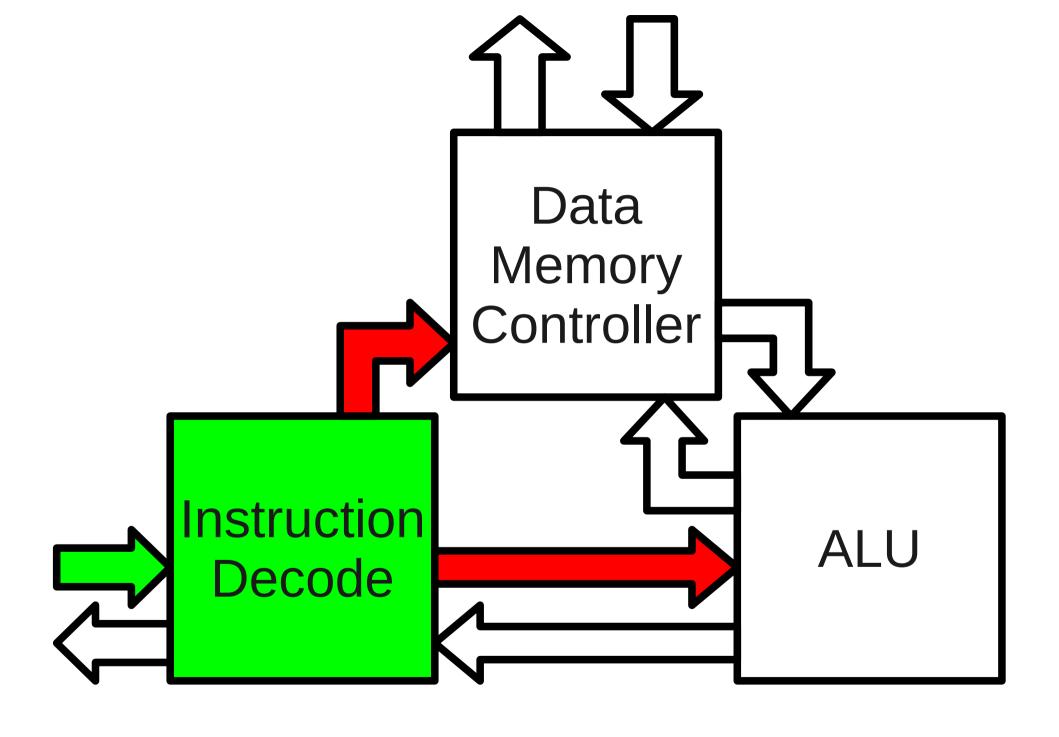
Functional development

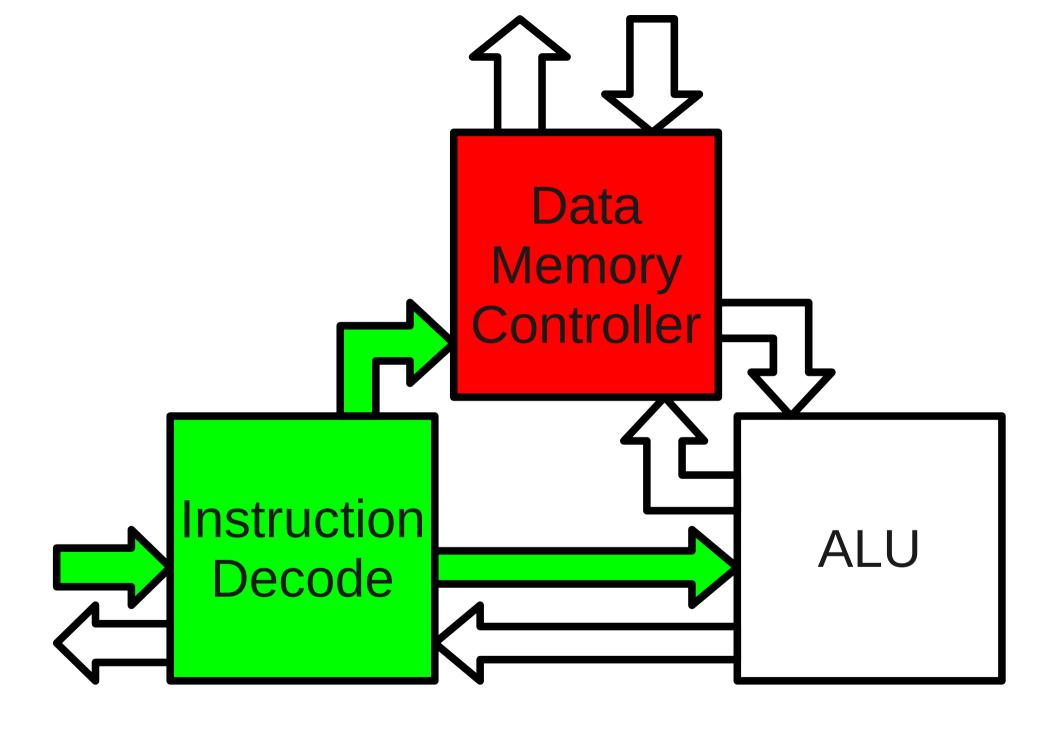
- 20 days to develop the synchronous version
- Desynchronised
 - Dual-rail early output
 - Wagging
- 10 days of tuning
 - Interesting stuff
- One man month processor
- 12 month of automating the process

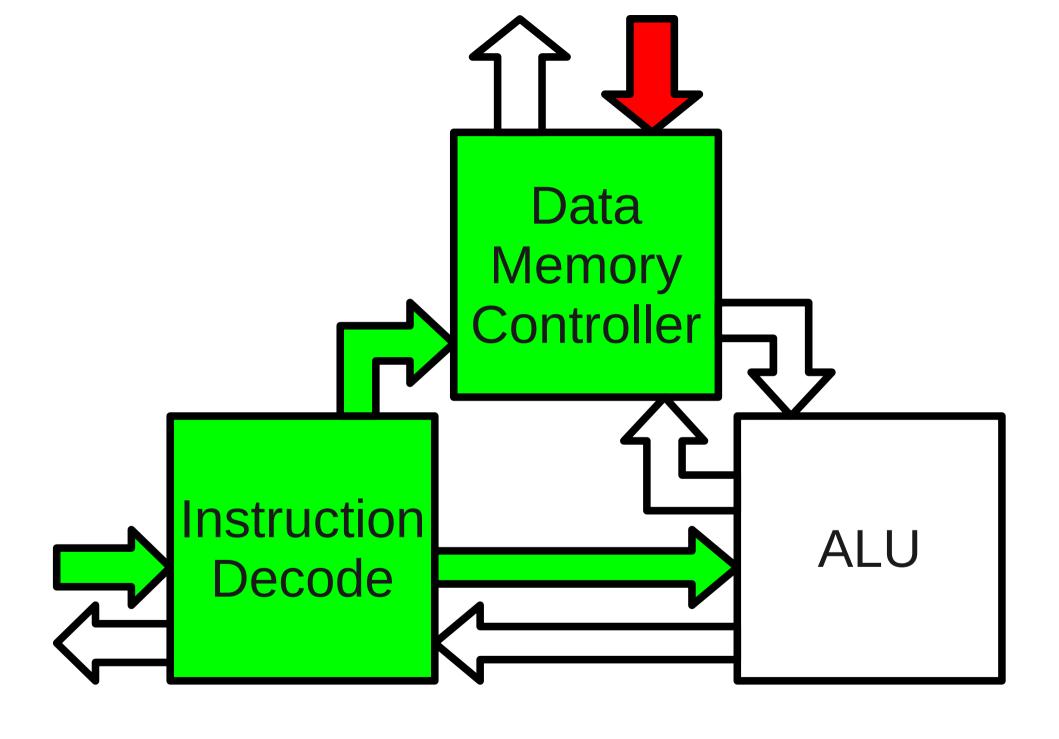


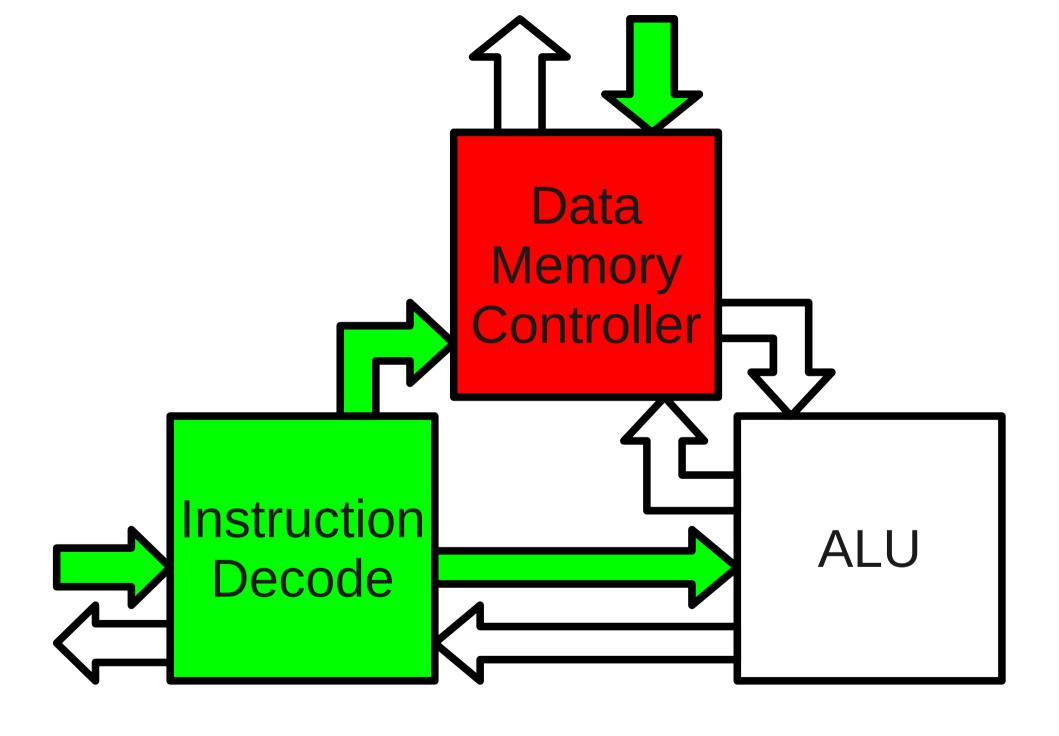


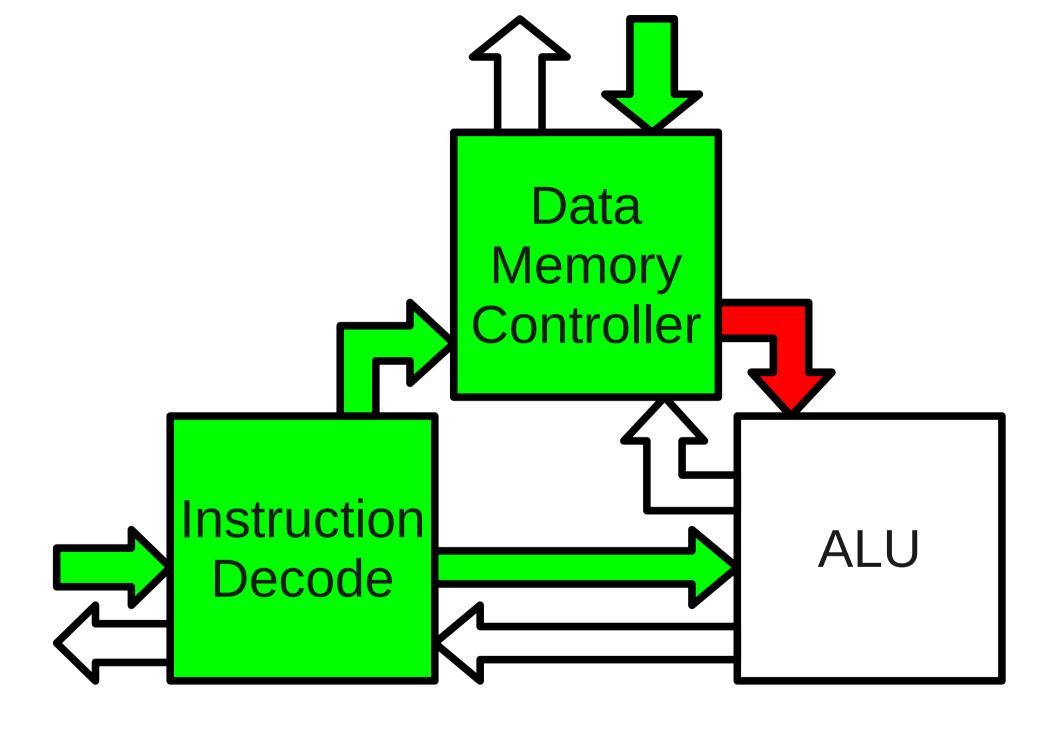


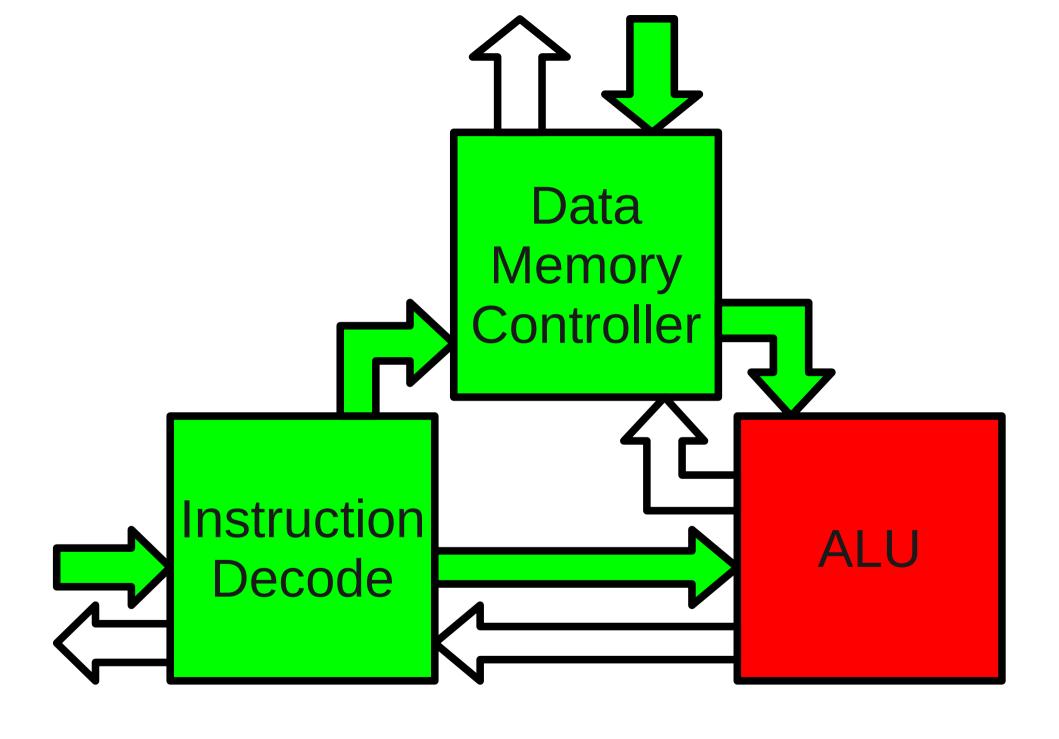


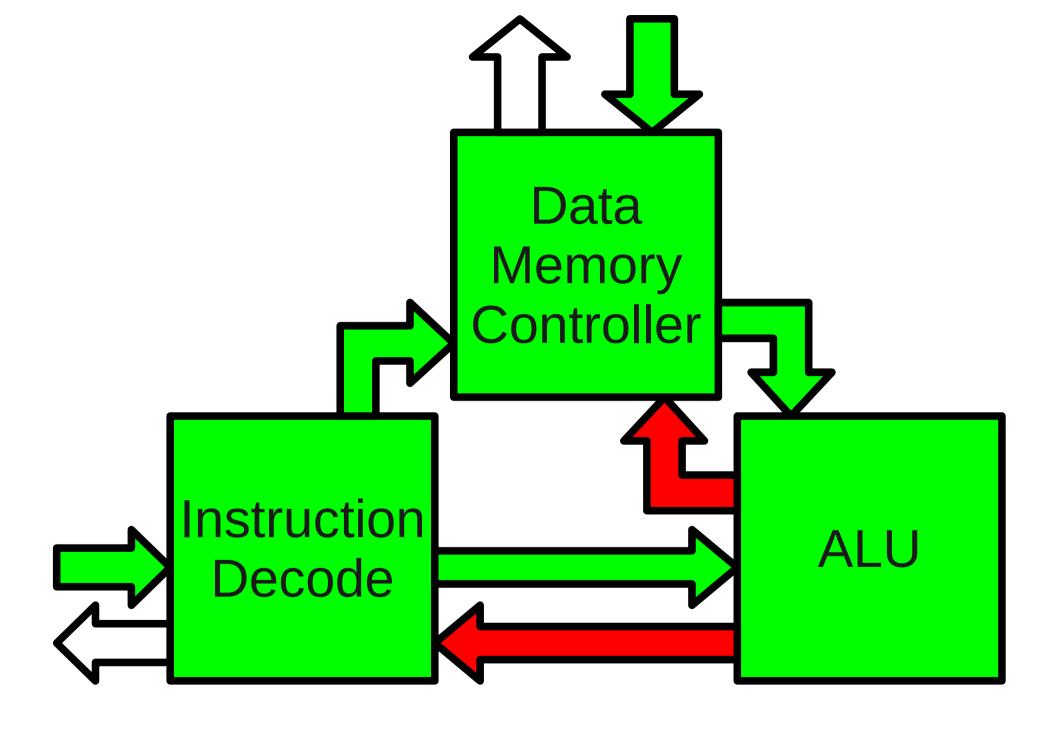


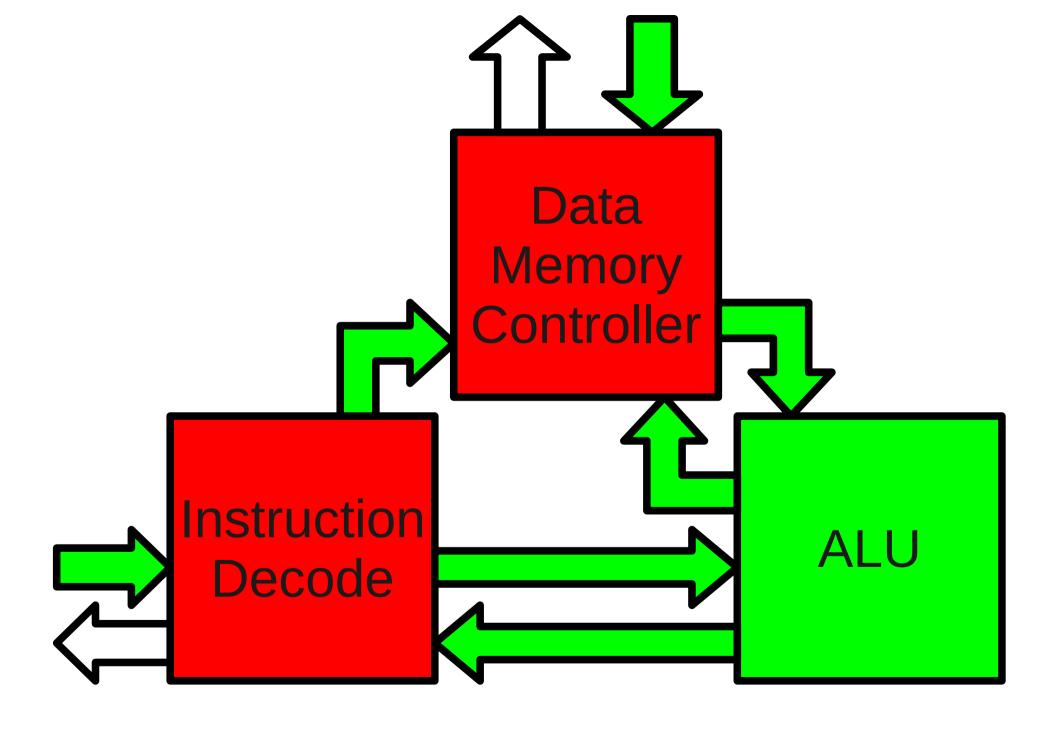


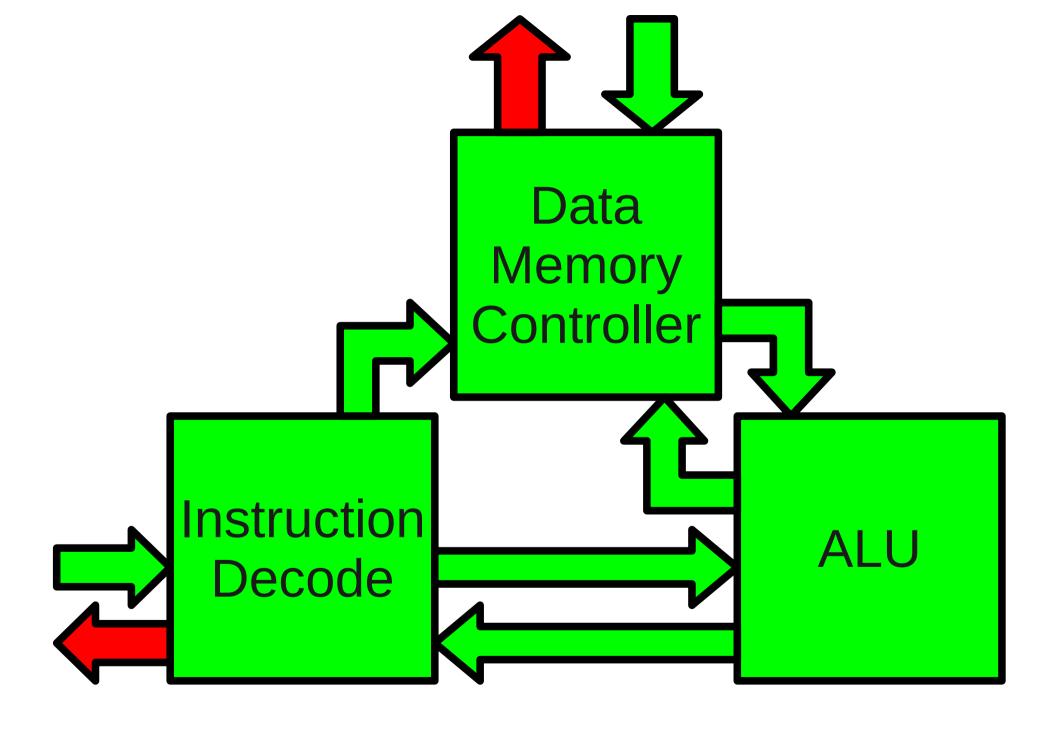






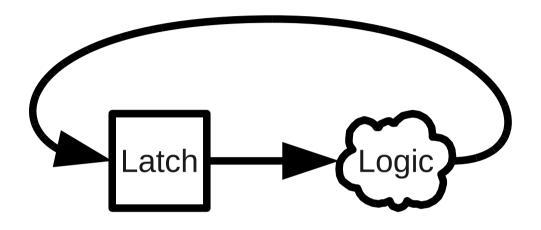


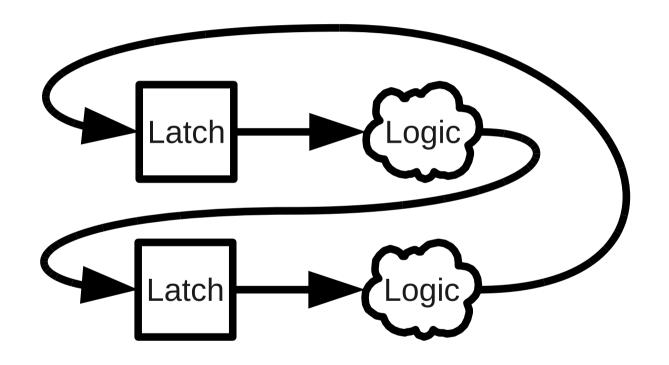


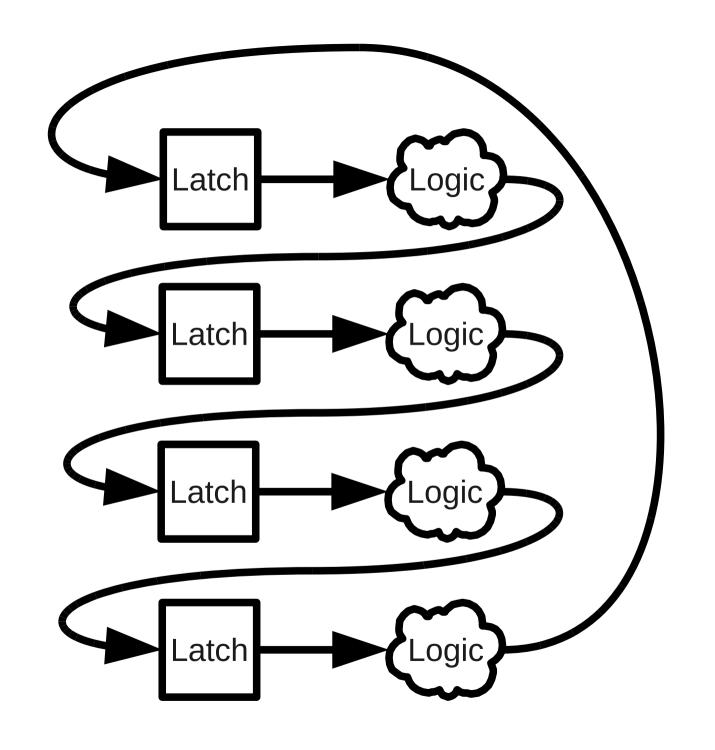


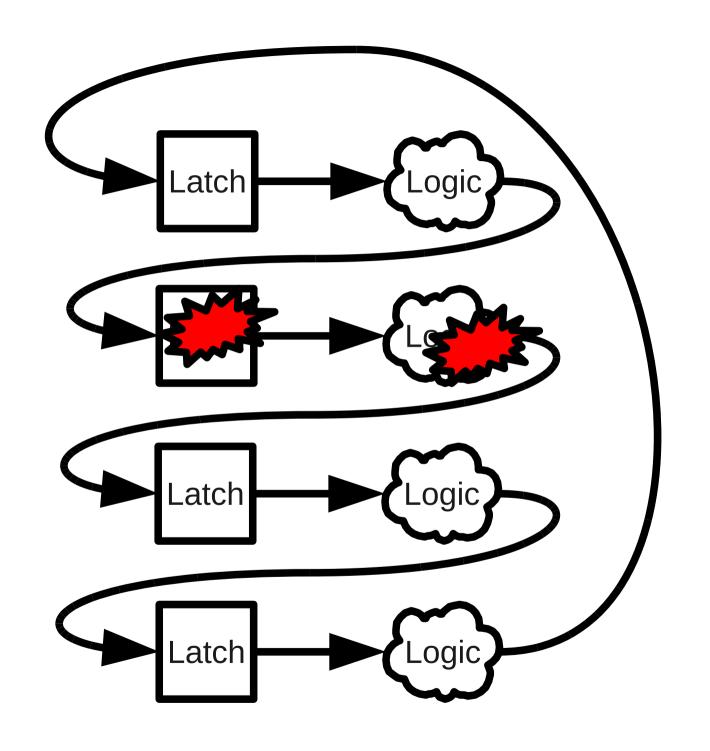
Performance wrapper

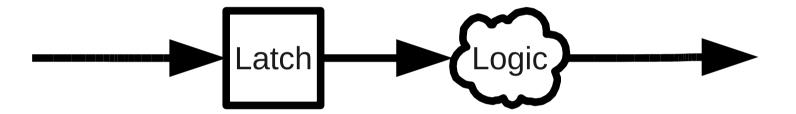
- Keep original structure and functional behaviour
- Design should remain functional in its synchronous form
- Wagging
 - With by-passable stages
- Add pipelining
- Add caching
 - Instruction cache
 - Data cache

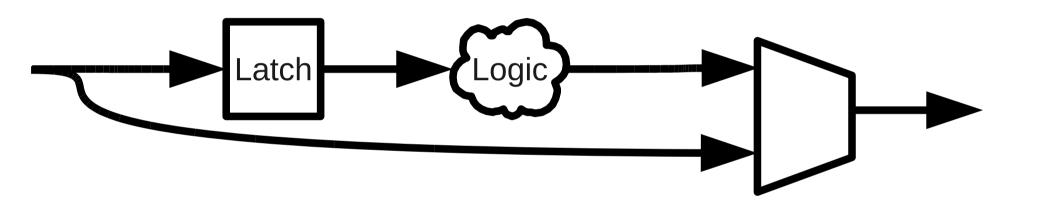


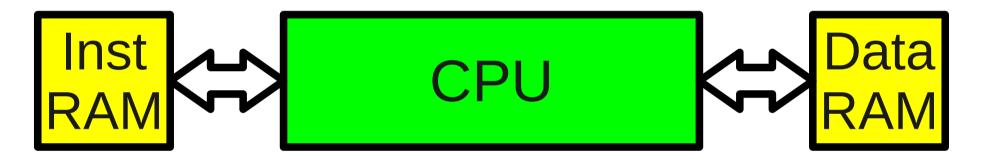


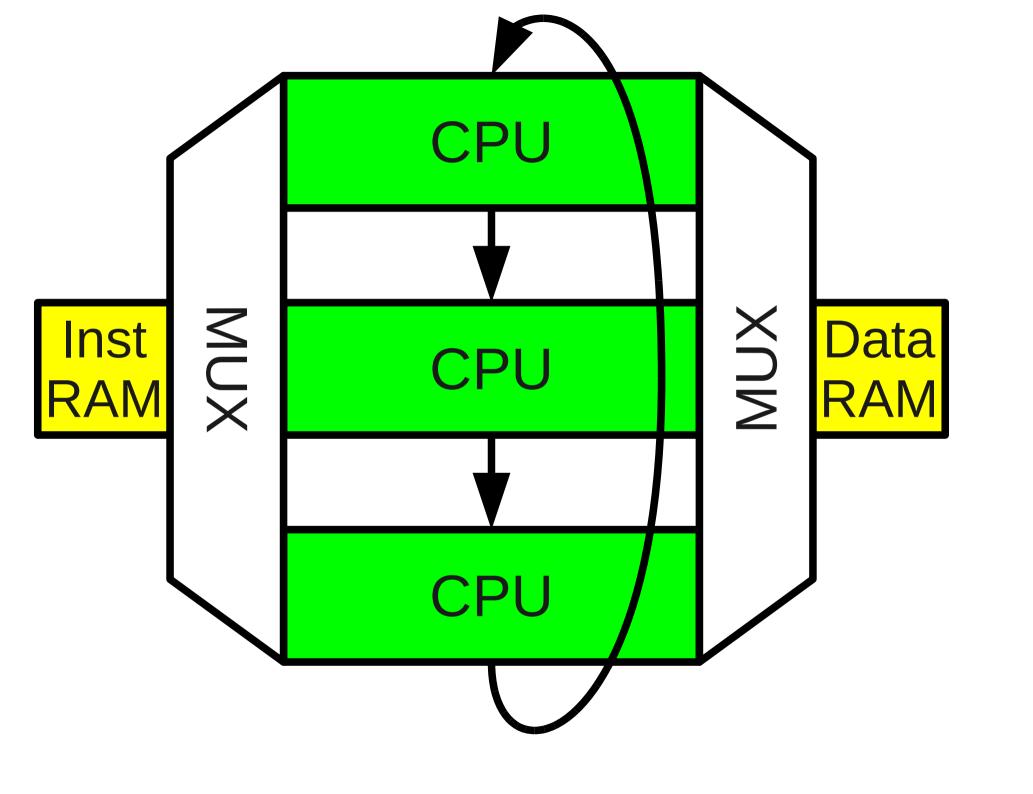


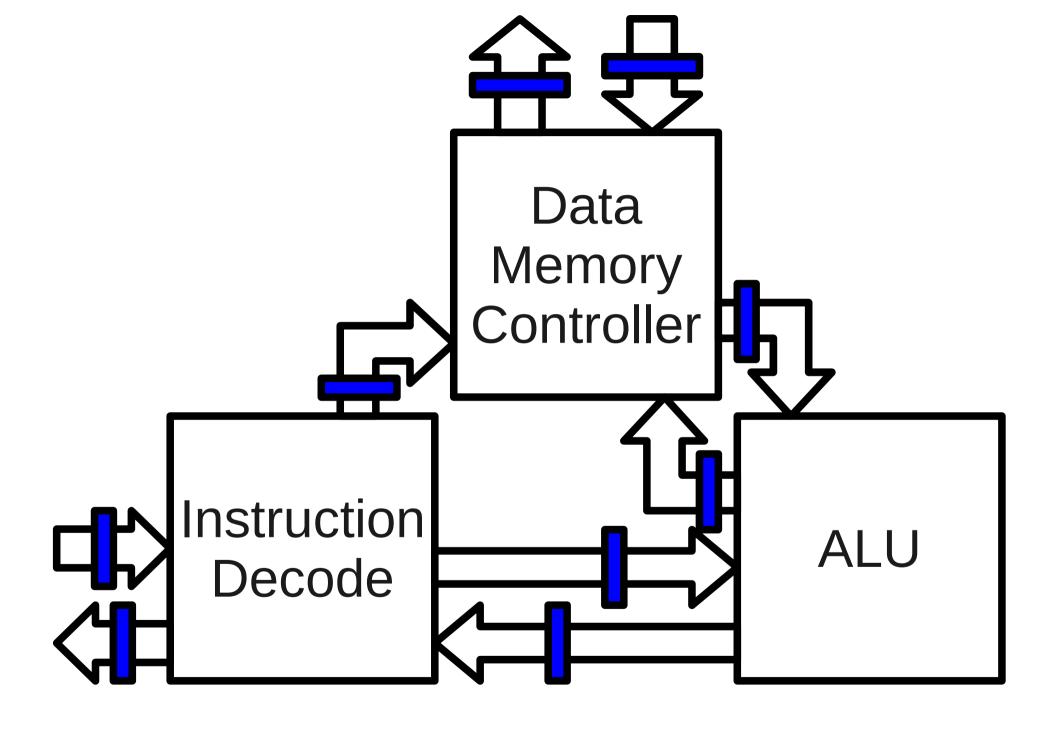


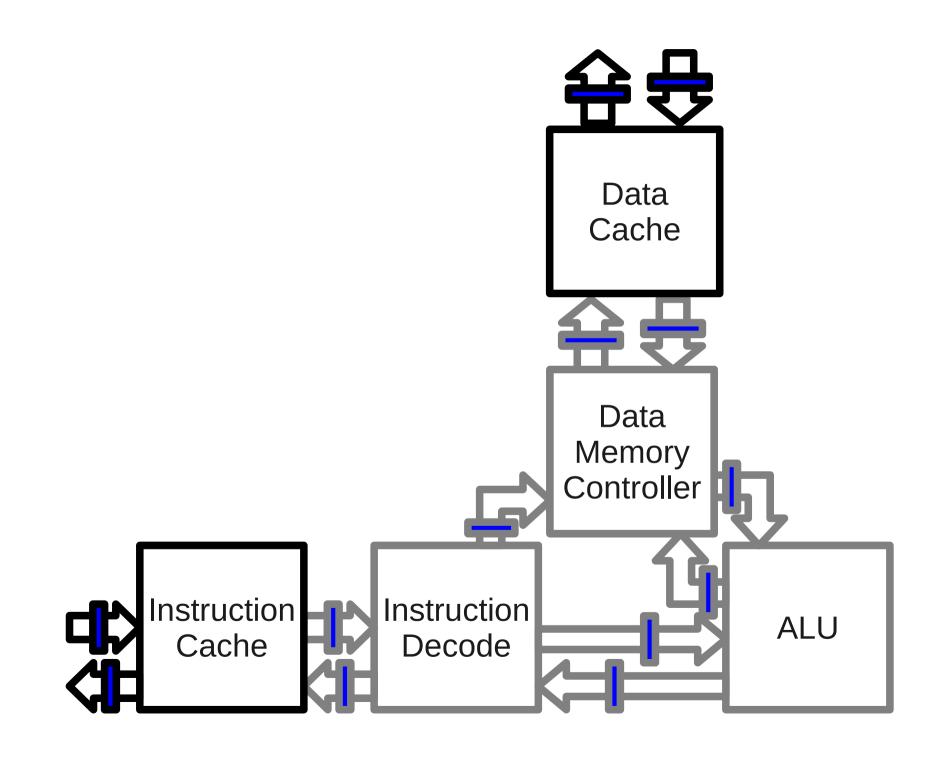




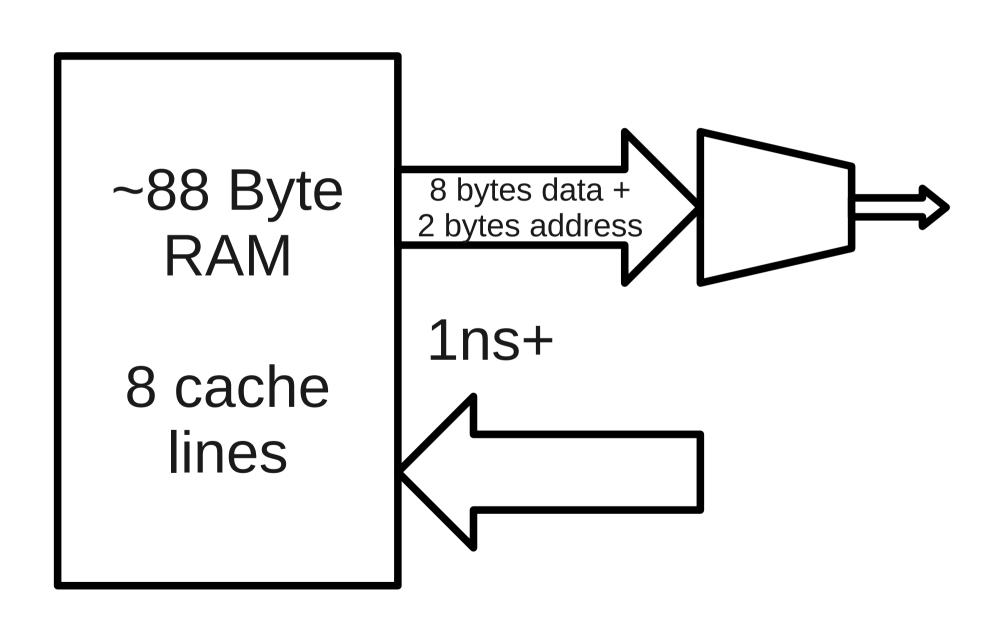




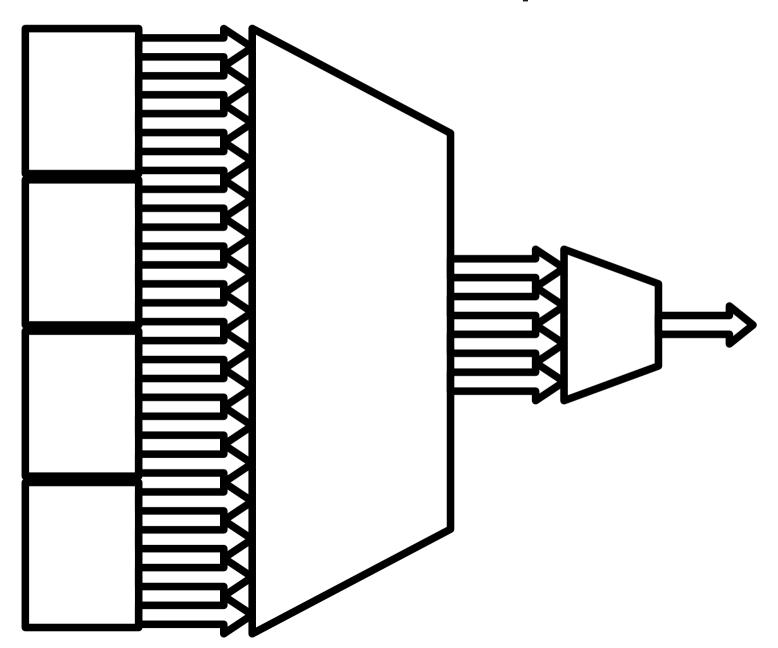




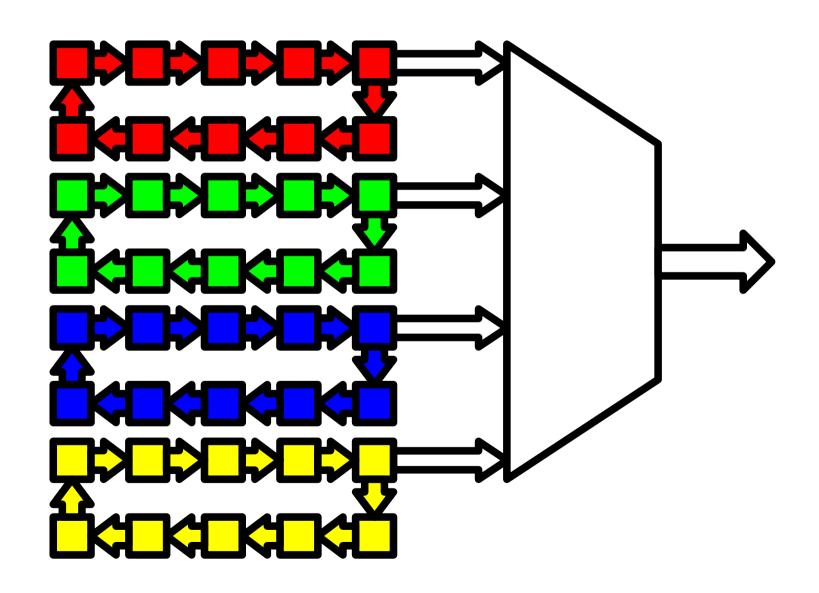
Instruction cache option 1



Instruction cache option 2



Instruction cache option 3

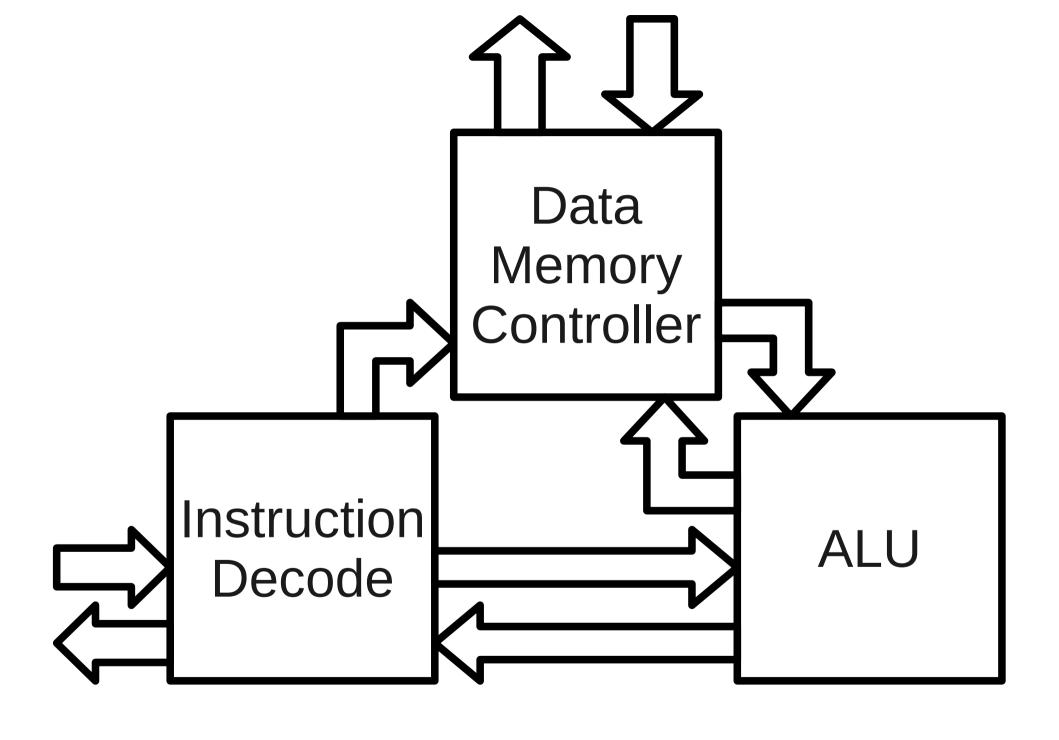


Data cache

- Register bank cache
 - 8 registers
 - Stack Pointer
- 2 entry stack cache
 - Snoops instruction stream
 - Detects push and call operations
 - Flushes one entry
 - Allows all instructions to execute in one cycle per instruction stream byte read

Comparisons (How to cheat)

- Handshake solutions
 - State performance in MHz equivalent
 - 60.5 MHz Woot!
 - 6 MIPS
 - ~100 times faster
- Caltech
 - Only measure the performance of 2 instructions
 - Accumulate and NOP
 - Don't memory map the accumulator
 - ~100 MIPS



Tape-out

- Implemented in 130nm tech
- 1st tape-out was "cancelled"
- 2nd tape-out 22nd of November